Eran Cohen

(US citizen)
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Work History:

NFTI Corp. Jul/02-Now (Consulted for Texas Instruments (Twice), Intel, Broadcom (Twice), MentorGraphics, Lecroy, Rosum , FyreStorm, Ambarella (Twice), Altierre, Novafora, EnvisionTech, IPSIL, OcarinaTech, Exalt Communications, IncelVision, W5 Networks, and others)
Morphics Technology Inc. Mar/2001-Jun/2002
PC-Tel Inc. Dec/1998-Feb/2001
ITeX Inc. Jan/1998-Nov/1998
Terayon Communications Systems Dec/1994-Jan/1998
AT&T Bell Labs Nov/1992-Nov/1994
National Semi Conductor Feb/1986-Nov/1992

Experience/Accomplishments:

- Completed numerous chips from concept to production: Communications, DSP, PHY, Video, and other applications. Had hands on key roles driving all aspects of ASIC and FPGA development. Self starter and independent.
- Lots of hands on experience with ASIC or FPGA (Xilinx, Altera): architecture, design, verification, synthesis, STA, DFT, formal verification, FPGA prototyping, bring up, etc. Lots of recent experience with low power designs.
- Interacted tightly with internal and external COT groups on floor plan, static timing, place & route, etc.
- Implemented and verified an extremely low power complex rendering engine and LCD controller.
- Designed and verified CFR (Crest Factor Reduction) and DPD (Digital PreDistortion) blocks for a wireless infrastructure ASSP. Both blocks are about 3M gates together, and made about ½ of the ASIC. Lots of attention was given to low power.
- Integrated Bluetooth Physical layer into Bluetooth protocol analyzer.
- Added IP protection to an Arm based sophisticated audio filtering system.
- Participated in the design of UWB (Wireless USB) Modem (ASIC), back-haul wireless transceiver (Altera Startix 3), multi gigabits TCP/IP DDR HW (Xilinx Virtex), RFID and Graphic processor chipset, SW defined Video processor chip, & more.
- Led the development of a 14M gate - 245MHz chip for 3GPP cellular base stations in Morphics.
- Architected and developed an FPGA (Xilinx Virtex 2Pro) and a board for a positioning system based on DTV signals.
- Developed test plan and executed the verification of major blocks of an H.264/MPEG/JPEG Encoder/Decoder ASIC.
- Architected, implemented and verified 2 broadband ADSL/V.90 ASICs and FPGA prototypes (Various Xilinx Virtex families) and boards in PC-Tel.
- Represented PC-Tel in the ACR specification development committee.
- Led the development of a 1M gate ADSL chip, which became the top seller of ITeX, and enabled it going public.
- First engineer to join Terayon Communication systems. Had a key role in developing the multimedia cable modem system concept (Algorithms, Software, Hardware & RF), including technical interaction with customers.
- Architected an S-CDMA (DOCSIS 1.2) cable Modem ASIC, and led its micro-architecture development, design, verification, DFT, bring up and SW and HW integration into a shipping product, which enabled Terayon to go public.
- Developed road map and detailed architecture, and wrote and maintained a detailed functional and design specification for most of the above ASICs, including DFT and bringing up the test vectors on the ATE (BIST, scan, IDDQ, etc.).
- Architected and implemented the Signal Processing Engine, the heart of a very successful xDSL modem chip set developed in AT&T Bell Labs department, which was later spun off as Globe Span.
- Conducted DSP simulations and LAN modeling, and led the system engineering of a fast transceiver for LAN applications (100/10Mbps Ethernet, FDDI, and ATM). Filed 2 related patents.
- Designed a chip-set for 100/10Mbps fast Ethernet transceiver.
- Participated in IEEE 802.3 standards committee and its High Speed and 10GBE working groups. Co-authored patents.
- Architected the digital chip for 10GB Ethernet over copper w/ XAUI & XFI I/F, and 1GB mode w/ GMII I/F. - Implemented a voice band modem transmitter and echo canceller.
- Implemented a UDP/TCP/IP TOE in FPGA (Xilinx Virtex), which could reach Tera bits per second.
- Participated in the development and verification of various CISCs & DSPs in National Semi Conductor.

Education:

- MSEE, 1988 – Technion, Israel.
- BSCE, 1985 (Cum Laude) – Technion, Israel.

Other Design tools & Skills:

Verilog RTL, SystemVerilog, PLI, Synopsys, BC, Behavioral Synthesis, VCS, NC-Verilog, Vericov, Covermeter, Prime-time, Spyglass, Synplicity, ISE, Quartos, ChipScope, signalScan, Ambit (BuildGates), Verplex/Tuxedo, Cadence/SPW, Matlab, Verisity/Specman, Vera, SyetemVerilog, Tetramex, Mentor/Fastscan, Syntest, HDL-Score, TransEDA, AtHDL, Novas Debussy & Verdi, Virsim, Orcad, Unix/Solaris, Windows, C, Assembler, Xilinx Virtex, Altera Stratix-III, Arm, AMBA, AHB, Microblaze, OpenRisc, DW8051, master/target PCI bus, DMA, Codec I/F, DDR1, DDR2, DDR3, FEC (ReedSolomon, Trellis, Viterbi), modulation (CAP, QAM, CAP, OFDM), DSP (FFT, IFFT, FIR, IIR, Bi-Quad, raised cosine shaping filters, matched filters, Decimation, Interpolation, Carrier recovery, Clock recovery, AGC, blind/noise predictive/adaptive equalizers, THP), wireless, G.lite, G.dmt, SAR, SERDES, 802.11, 802.16, WiFi, WiMAX, Bluetooth, CFR, DPD, PAL, NTSC, ATSC.